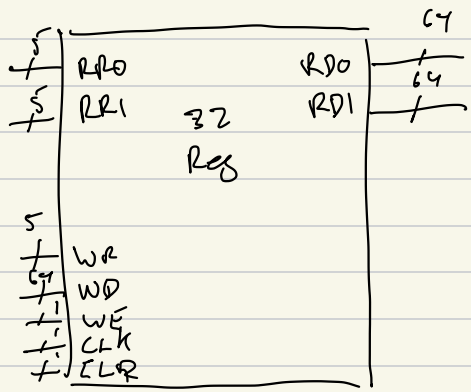
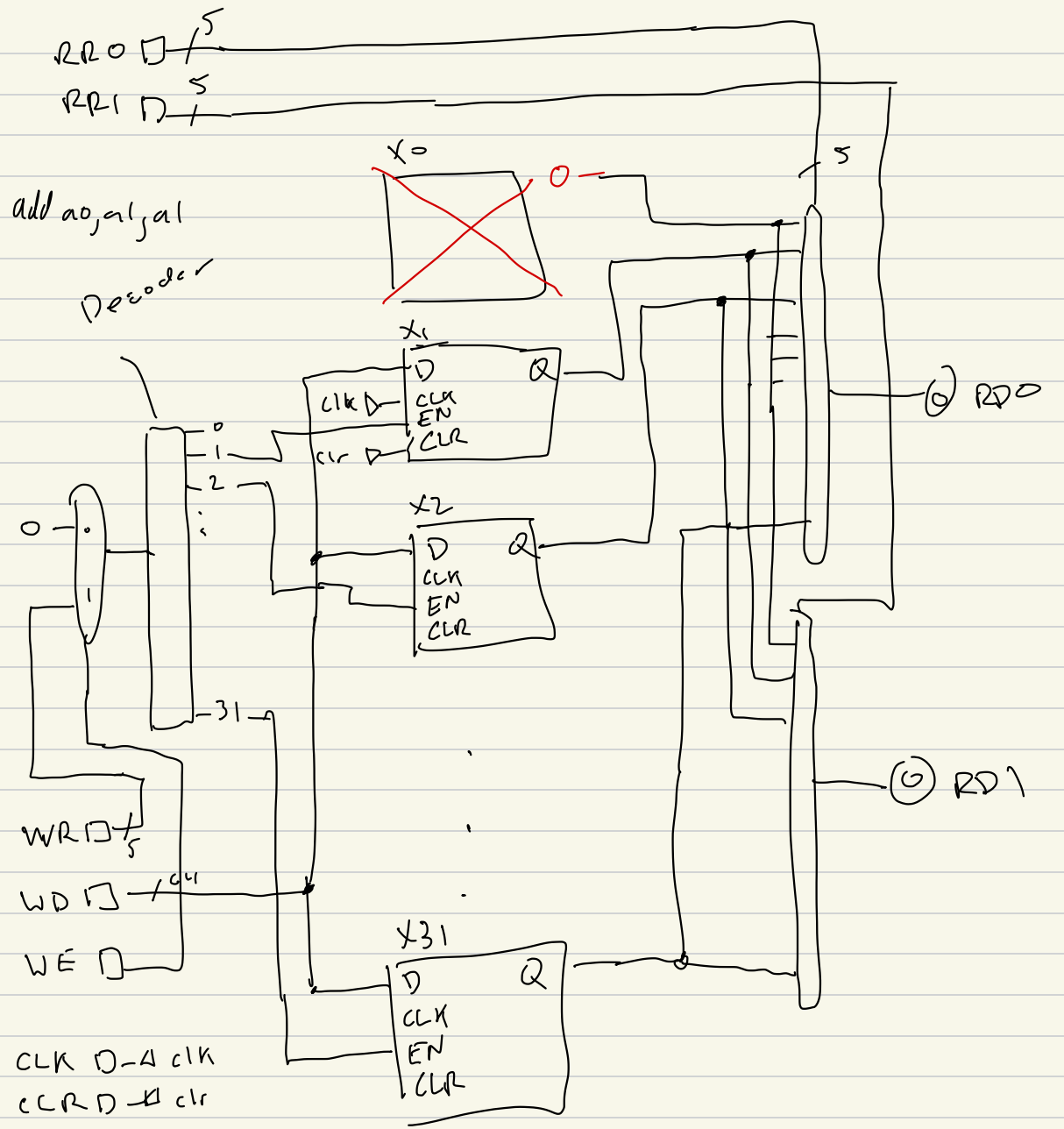
Register File



RR - read reg #
RD - read data value

WR - write reg
WD - write data
WE - write enable

On a single clock cycle
1) read up to two reg values
2) write at most one reg


RR0
5
RR1
5
X0
0
5
add a0,a1,a1
Decoder
X1
D
Q
CLK
EN
CLR
clk
clr
0
1
2
31
X2
D
Q
CLK
EN
CLR
0
1
RD0
RD1
WR
5
WD
clk
WE
X31
D
Q
CLK
EN
CLR
CLK
clk
CLR
clr

ALU Arithmetic Logic Unit